Amendments to the Claims

LISTING OF CLAIMS

Claims 1-75 (canceled)

76. (previously presented) A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side and a thickness, the dice comprising a plurality of die contacts;

forming a plurality of polymer filled trenches on the first side between the dice having a depth less than the thickness;

forming a plurality of conductive vias in the dice in electrical communication with the die contacts;

thinning the substrate from the second side to the polymer filled trenches;

forming a plurality of grooves through the polymer filled trenches to singulate the dice; and

forming a plurality of terminal contacts on the dice in electrical communication with the conductive vias.

77. (previously presented) The method of claim 76 wherein the forming the terminal contacts step comprises etching the substrate to expose portions of the conductive vias.

78. (previously presented) The method of claim 76 further comprising exposing tip portions of the conductive vias and forming the terminal contacts on the tip portions.

79. (previously presented) The method of claim 76 wherein the forming the conductive vias step comprising laser machining openings in the substrate, and at least partially filling the openings with a conductive material.

80. (previously presented) The method of claim 76 wherein the forming the conductive vias step comprises implanting a dopant on portions of the substrate and forming the conductive vias on the portions.

81. (previously presented) The method of claim 76 further comprising forming a first polymer layer on the first side, and a plurality of first contact bumps in the first polymer layer in electrical communication with the conductive vias.

82. (previously presented) The method of claim 76 further comprising forming a second polymer layer on the second side, and a plurality of contact bumps in the second polymer layer in electrical communication with the conductive vias, and then forming the terminal contacts on the contact bumps.

83. (previously presented) The method of claim 76 wherein the thinning the substrate step is performed by planarizing the substrate.

84. (previously presented) The method of claim 76 wherein the thinning the substrate step is performed by planarizing and then etching the substrate.

85. (previously presented) The method of claim 76 wherein the thinning the substrate step is performed by etching the substrate.

86. (previously presented) The method of claim 76 wherein the forming the grooves step is performed by sawing through the polymer filled trenches.

87. (previously presented) The method of claim 76 wherein the forming the grooves step is performed by etching through the polymer filled trenches.

88. (previously presented) The method of claim 76 wherein the forming the polymer filled trenches is performed by scribing the substrate with a plurality of trenches and then filling the trenches with a polymer material.

89. (previously presented) The method of claim 76 wherein the forming the polymer filled trenches is performed by etching the substrate with a plurality of trenches and then filling the trenches with a polymer material.

Claim 90 (canceled)

91. (previously presented) A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a substrate having a first side, a second side and a thickness, the dice comprising a plurality of die contacts;

forming a plurality of conductive vias in the dice in electrical communication with the die contacts;

forming a plurality of polymer filled trenches in the substrate then thinning the substrate from the second side to expose the polymer filled trenches;

etching the substrate to expose portions of the conductive vias;

forming a plurality of grooves through the polymer filled trenches to singulate the dice; and

forming a plurality of terminal contacts on the dice in electrical communication with the conductive vias.

92. (previously presented) The method of claim 91 further comprising forming a back side polymer layer on the second side.

93. (previously presented) The method of claim 92 wherein the polymer layer comprises parylene.

94. (previously presented) The method of claim 91 further comprising forming contact bumps on the die contacts.

95. (previously presented) The method of claim 91 further comprising forming a front side polymer layer on the first side.

96. (previously presented) The method of claim 95 further comprising forming planarized contact bumps in the front side polymer layer and on the die contacts.

97. (previously presented) A method for fabricating semiconductor components comprising:

providing a semiconductor substrate comprising a plurality of semiconductor dice having a plurality of die contacts, the substrate having a first side, a second side and a thickness;

forming a plurality of trenches on the first side along peripheral edges of the dice, each trench having a depth less than the thickness;

forming a plurality of contact bumps on the die contacts;

forming a plurality of conductive vias in the substrate in electrical communication with the contact bumps;

forming a first polymer layer on the contact bumps and in the trenches to form polymer filled trenches;

thinning the substrate from the second side to expose the polymer filled trenches; and

singulating the dice through the trenches such that each component includes a semiconductor die covered on at least five sides by a portion of the first polymer layer, and portions of the polymer filled trenches.

98. (previously presented) The method of claim 97 further comprising forming a second polymer layer on the second side, and forming a plurality of terminal contacts on the second polymer layer in electrical communication with the conductive vias.

99. (previously presented) The method of claim 97 further comprising etching the substrate following the thinning step such that the substrate is recessed with respect to the portions of the polymer filled trenches.

100. (previously presented) The method of claim 97 further comprising etching the substrate following the thinning step to form the conductive vias as pins in a pin grid array or micro pin grid array.

101. (previously presented) The method of claim 97 further comprising etching or grinding the portions of the polymer filled trenches such that the portions are recessed with respect to the substrate.

102. (previously presented) The method of claim 97 further comprising forming a plurality of second contact bumps in the second polymer layer in electrical communication with the conductive vias and then forming the terminal contacts on the second contact bumps.

103. (previously presented) The method of claim 97 wherein the conductive vias comprise openings in the

substrate, insulating layers on the openings and a conductive material in the openings.

104. (previously presented) The method of claim 97 wherein the conductive vias comprise portions of the substrate implanted with a dopant.

105. (previously presented) A method for fabricating semiconductor components comprising:

providing a plurality of semiconductor dice on a semiconductor substrate having a circuit side and a back side;

forming a plurality of trenches along peripheral edges of the dice part way through the substrate;

depositing a polymer material in the trenches;

forming a plurality of contact bumps on the dice;

forming a first polymer layer on the circuit side and the contact bumps;

forming a plurality of conductive vias in the dice in electrical communication with the contact bumps;

thinning the substrate from the back side to contact the polymer material in the trenches and to thin the back side;

forming a plurality of terminal contacts on the back side or on the circuit side in electrical communication with the conductive vias; and

singulating the dice by forming grooves through the trenches and the polymer material.

106. (previously presented) The method of claim 105 further comprising forming a second polymer layer on the back side and forming a plurality of second conductive vias in the second polymer layer in electrical communication with the conductive vias.

107. (previously presented) The method of claim 105 further comprising forming a plurality of second contact bumps on the back side following the thinning step in electrical communication with the conductive vias, and forming the terminal contacts on the contact bumps.

108. (previously presented) The method of claim 105 wherein the forming the conductive vias step comprises laser machining openings and at least partially filling the openings with a conductive material.

109. (previously presented) The method of claim 105 wherein the forming the conductive vias step comprises implanting a dopant into a selected portion of the substrate.

110. (previously presented) The method of claim 105 wherein the thinning the substrate step comprises mechanically planarizing the substrate.

111. (previously presented) The method of claim 105 wherein the contact bumps and the first polymer layer have a planarized surface.

112. (previously presented) The method of claim 105 wherein the thinning the substrate step comprises mechanically planarizing then etching the substrate.

113. (previously presented) The method of claim 105 wherein the thinning the substrate step comprises etching the substrate.

Claims 114-260 (canceled)